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DIGITAL/ANALOG CONVERTER AND CONTROL DEVICE USING THIS CONVERTER

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[There are no amendments to this patent.]

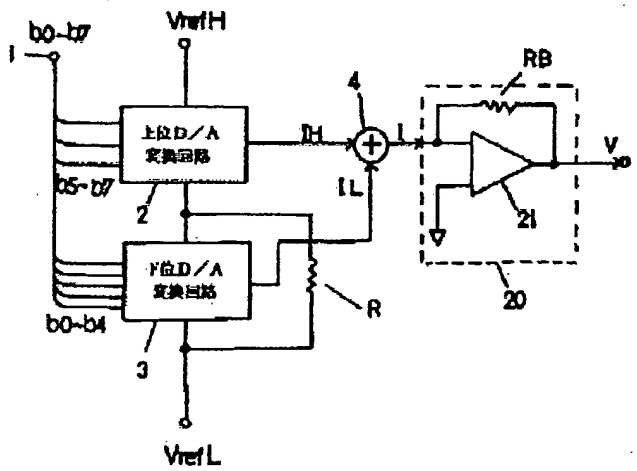
Abstract

Objective

To provide a segment type digital/analog converter at low cost and with high control accuracy, and a highly accurate control device using this converter.

Means to solve

Digital data having plural bits b0-b7 are divided into two or more segments. Digital/analog converting means 2, 3 for the segments are used to perform digital/analog conversion for the digital data of each of the aforementioned segments. The outputs of converting means 2, 3 are synthesized. For converting means 2, 3, the differential nonlinear error is within 1 LSB. The full scale of converting means 2 is greater than or equal to a value calculated by dividing the full scale of converting means 3 provided for the segment including the bit that is one order higher than the most significant bit of the other segment by 2^n (here, n is the number of bits of the segment, which is 3).



Key: 2 Upper D/A converting circuit
3 Lower D/A converting circuit

Claims

1. A digital/analog converter characterized by the following facts: digital data having plural bits are divided into two or more segments; a digital/analog converting means for segments is used to perform digital/analog conversion for the digital data of each of the aforementioned segments; the outputs of the aforementioned digital/analog converting means for the segments are synthesized; in this digital/analog converter,

for the aforementioned digital/analog converting means for segments, the differential nonlinear error is within 1 LSB; the full scale of the aforementioned digital/analog converting means for segments is greater than or equal to a value calculated by dividing the full scale of the aforementioned digital/analog converting means for segments provided for the segment including the bit one order higher than the most significant bit of the other segment by 2^n (here, n is the number of bits of the segment).

2. A control device characterized by the fact that it uses a comparison means to compare the output of the digital/analog converter described in Claim 1 with a reference signal and controls the aforementioned digital/analog converter based on the comparison output.

3. A control device characterized by the following facts: a voltage-control oscillator is connected to the digital/analog converter described in Claim 1; the oscillation frequency of the aforementioned voltage-control oscillator is compared with a reference frequency using a phase comparison means; the aforementioned digital/analog converter is controlled based on the comparison output; in this way, the aforementioned voltage-control oscillator is controlled.

Detailed explanation of the invention

[0001]

Industrial application field

The present invention pertains to a segment type digital/analog converter (referred to as a D/A converter hereinafter). In particular, the present invention pertains to a D/A converter that can effectively maintain its output consistent with a prescribed reference value, and to a control device using the aforementioned D/A converter.

[0002]

Prior art

A conventional segment type D/A converter will be explained based on Figures 6 and 7. Figure 7 is the block diagram of the conventional D/A converter. Digital data having the 8 bits b0-b7 are input from input terminal 1. b0 is the least significant bit, and b7 is the most significant bit. The digital data having the 8 bits b0-b7 are divided into two segments of the lower bits b0-b4 and upper bits b5-b7.

[0003]

The upper bits b5-b7 are sent to upper D/A converting circuit 2. The lower bits b0-b4 are sent to lower D/A converting circuit 3. In this case, D/A converting circuits 2, 3 convert the input digital data into analog currents. For example, plural transistors are used as constant current sources. The currents corresponding to the input digital data are output from the constant current sources, added, and finally output.

[0004]

Upper D/A converting circuit 2 is connected to the constant voltage VrefH on the high voltage side. Lower D/A converting circuit 3 is connected to upper D/A converting circuit 2. Lower D/A converting circuit 3 is connected to the constant voltage VrefL on the low voltage

side. A resistor RA is connected in parallel with lower D/A converting circuit 3. Resistor RA will be explained later.

[0005]

Power is supplied to upper and lower D/A converting circuits 2, 3 by constant voltages VrefH, VrefL, and these converting circuits perform D/A conversion for the input digital data. Upper D/A converting circuit 2 outputs current IH corresponding to the data represented by upper bits b5-b7. Lower D/A converting circuit 3 outputs current IL corresponding to the data represented by lower bits b0-b4. Currents IH and IL are synthesized by current synthesizer 4 to obtain current I.

[0006]

Current I is sent to integrator 20. Integrator 20 converts current I into voltage V. Integrator 20 is comprised of operational amplifier 21 and feedback resistor RB, and outputs voltage V as the product of current I and resistance RB. D/A converting circuits 2, 3 can be constituted with almost the same resistors or elements. Consequently, when segment type D/A converters are integrated, integration becomes easy because of the low deviation of the elements in the integrated circuit.

[0007]

When the current IL output from lower D/A converting circuit 3 and current IH output from upper D/A converting circuit 2 are synthesized, the voltage applied to lower D/A converting circuit 3 is adjusted in order to match the aforementioned 8-bit digital data of b0-b7. Resistance RA is set such that the result of adding 1 LSB to the full scale of current IL is consistent with the result of dividing the full scale of current IH by 2-cubed (that is, 8).

[0008]

In this case, 1 LSB is the result of deriving a value equivalent to the change of current when the digital data changes by 1, under the assumption that the current is output continuously from the full scales of currents IH, IL. In lower D/A converting circuit 3, since there are five lower bits b0-b4, 1 LSB is the result of dividing the full scale of current IL by the fifth power of 2 (that is, 32). In upper D/A converting circuit 2, there are three upper bits b5-b7. Taking into consideration the fact that there are five lower bits b0-b4, 1 LSB is the result of dividing the full scale of current IH by the eighth power of 2 (that is, 256). When the current is converted to voltage V by integrator 20, 1 LSB has the same definition.

[0009]

On the other hand, the result of dividing the full scale of current IH output from upper D/A converting circuit 2 by 2-cubed (that is, 8) is the result of deriving a value equivalent to the change in the output of D/A converter 3 when the least significant bit b5 among the upper bits b5-b7 has a change of 1 from the full scale of current IH output from D/A converting circuit 2.

[0010]

Figure 6 is the characteristic diagram of the output of the aforementioned D/A converter. When the input digital data is 0 (00000000 in binary), neither upper D/A converting circuit 3 nor lower D/A converting circuit 2 outputs current, and there is no current I. In other words, the output voltage V is 0. When the digital data is increased increments of 1 from 0, lower bits b0-b4 change as long as the data is 31 or less, and current IL is increased by lower D/A converting circuit 3. There is no change in the upper bits b5-b7. Current IL becomes current I. If lower D/A converting circuit 3 has good linearity, the relationship between digital data and current I becomes straight line 51.

[0011]

When the digital data is 31, the lower bits b0-b4 input into lower D/A converting circuit 3 all become 1 (11111 in binary), and the upper bits b5-b7 are all 0. When 1 is added to that digital data, since the binary number is carried, all the lower bits b0-b4 input into lower D/A converting circuit 3 become 0 (00000 in binary). Among the upper bits b5-b7 input into upper D/A converting circuit 2, only the least significant bit b5 becomes 1 (001 in binary).

[0012]

At that time, lower bits b0-b4 are inverted and upper bits b5-b7 are added for output voltage V. Usually, resistance RA varies, and output voltage V becomes non-continuous as shown at 52. Also, as the digital data is increased, all the lower bits b0-b4 will be inverted, and discontinuities 53, 54 tend to occur in the same way. The point at which all the lower bits b0-b4 are inverted is the switching point of the segments.

[0013]

Problems to be solved by the invention

As described above, even if D/A converting circuits 2, 3 for each segment have good linearity, since resistance RA usually varies, the output tends to become discontinuous at the switching point of each segment. The maximum difference between the ideal output voltage V and the actual output is called the differential nonlinear error. Even if the differential nonlinear

error in each segment is 1 LSB or less, it will exceed 1 LSB at the switching point of the segments. In particular, when output voltage V varies significantly in the positive direction at segment-switching point 53 shown in Figure 6, even if the voltage is controlled during the change, it is not possible to obtain a suitable output voltage V.

[0014]

Consequently, it is difficult to use a segment type D/A converter for a device that requires highly accurate control. In order to perform highly accurate control, it is necessary to use a highly accurate D/A converter with a differential nonlinear error within 1 LSB. Such a converter is expensive, however, and will increase the cost of the control device.

[0015]

The purpose of the present invention is to solve the aforementioned problem by providing a segment type D/A converter with low cost and high control accuracy as well as a control device using such a D/A converter.

[0016]

Means for solving the problems

In order to realize the aforementioned purpose, the first configuration of the present invention provides a digital/analog converter characterized by the following facts: digital data having plural bits are divided into two or more segments; a digital/analog converting means for segments is used to perform digital/analog conversion for the digital data of each of the aforementioned segments; the outputs of the aforementioned digital/analog converting means for the segments are synthesized; in this digital/analog converter, for the aforementioned digital/analog converting means for segments, the differential nonlinear error is within 1 LSB; the full scale of the aforementioned digital/analog converting means for segments is greater than or equal to a value calculated by dividing the full scale of the aforementioned digital/analog converting means for segments set up for the segment including the bit one order higher than the most significant bit of the other segment by 2^n (here, n is the number of bits of the segment).

[0017]

According to this configuration, digital data having plural bits are divided into two or more segments. The digital/analog converting means provided for each segment performs digital/analog conversion for each segment. The differential nonlinear error of the digital/analog converting means for each segment is within 1 LSB.

[0018]

The full scale of the digital/analog converting means for each segment is greater than or equal to a value calculated by dividing the full scale of the digital/analog converting means for segments provided for the segment including the bit one order higher than the most significant bit of the segment by 2^n (here, n is the number of bits of the segment). In this way, the differential nonlinear error of the digital/analog converter is kept within 1 LSB in the positive direction.

[0019]

A large error may also occur in the negative direction. However, since the error in the positive direction is less than 1 LSB, when the converter is used for a control to match a certain reference voltage, the voltage output from digital/analog converter can be controlled at an accuracy within 1 LSB. Since deviation in the negative direction is not restricted, it is unnecessary to perform fine adjustments to match the current output by the digital/analog converter for segments. The cost is therefore low.

[0020]

In the second configuration of the present invention, the output of the digital/analog converter with the aforementioned first configuration is compared with a reference signal by a comparison means, and the aforementioned digital/analog converter is controlled based on the comparison output.

[0021]

According to this configuration, the output of the digital/analog converter is compared with a reference signal by a comparison means. The aforementioned digital/analog converter is controlled based on the comparison output. As a result of this control, the output of the digital/analog converter is maintained at the same value as the reference signal.

[0022]

Since the differential nonlinear error of the digital/analog converter is less than 1 LSB in the positive direction, the output can be constantly controlled at an accuracy within 1 LSB of the set output value. A highly accurate control device can be obtained in this way.

[0023]

In the third configuration of the present invention, a voltage-control oscillator is connected to the digital/analog converter with the aforementioned first configuration. The

oscillation frequency of the aforementioned voltage-control oscillator is compared with a reference frequency by a phase-comparison means. The aforementioned digital/analog converter is controlled based on the comparison output. The aforementioned voltage-control oscillator is controlled in this way.

[0024]

According to this configuration, the output of the digital/analog converter is input into the voltage-control oscillator. The voltage-control oscillator can control frequency depending on the voltage output from the digital/analog converter. The oscillation frequency is increased along with the voltage.

[0025]

The oscillation frequency and the reference frequency are compared by a phase comparison means. If the oscillation frequency is different from the reference frequency, the output of the digital/analog converter is changed to make the oscillation frequency of the voltage-control oscillator approach the reference frequency. On the other hand, if the oscillation frequency is the same as the reference frequency, the oscillation frequency is fixed. In this way, the oscillation frequency can be kept the same as the reference frequency.

[0026]

Embodiment of the invention

<First embodiment>

The first embodiment of the present invention will be explained based on Figures 1 and 2. Figure 1 is a block diagram illustrating an embodiment of the D/A converter disclosed in the present invention. Since it has the same configuration as the conventional example shown in Figure 7 except for the resistance of resistor R, the same parts as those of the aforementioned conventional D/A converter (Figure 7) are represented by the same symbols, respectively, and will not be explained again. Upper D/A converting circuit 2 performs D/A conversion for the three upper bits b5-b7, while lower D/A converting circuit 3 converts the five lower bits b0-b4. However, it is also possible to change the number of bits subjected to the D/A conversion performed by D/A converting circuits 2 and 3.

[0027]

The digital data can also be divided into 3 or more segments. Also, the number of bits of digital data is not limited to 8. The differential nonlinear error is within 1 LSB for both upper D/A converting circuit 2 and lower D/A converting circuit 3.

[0028]

In the conventional example, as described above, resistance RA adds 1 LSB to the full scale of the current IL output from lower D/A converting circuit 3. It is set to be consistent with the current change when the least significant bit b5 of upper D/A converting circuit 2 is changed by 1. On the other hand, in this embodiment, the full scale of lower D/A converting circuit 3 is greater than or equal to a value calculated by dividing the full scale of upper D/A converting circuit 2 by 2 raised to a power equal to the number of upper bits b5-b7 (that is, 8, as the cube of 2).

[0029]

Figure 2 is the characteristic diagram of the D/A conversion of the D/A converter disclosed in this embodiment. If the input digital data is 0, neither upper D/A converting circuit 2 nor lower D/A converting circuit 3 has current output, and there is no current I. In other words, the output voltage is 0. When the digital data is increased 1 at a time from 0, lower bits b0-b4 change as long as the data is less than 31, and current IL corresponding to the digital data is output by lower D/A converting circuit 3. There is no change in the upper bits b5-b7, and there is no current IH. Current IL becomes current I. If lower D/A converting circuit 3 has good linearity, the relationship between digital data and current I becomes straight line 11.

[0030]

At segment-switching point 12, the full scale of lower D/A converting circuit 3 becomes greater than or equal to a value calculated by dividing the full scale of upper D/A converting circuit 2 by 2-cubed (that is, 8). As a result, the output current I becomes smaller or larger. The difference is within 1 LSB. Similarly, at segment-switching points 13, 14, the output voltage V of the D/A converter rises or drops. However, the output difference will not exceed 1 LSB.

[0031]

As described above, the differential nonlinear error in the positive direction of the D/A converter of the present invention is within 1 LSB in any part. Since the differential nonlinear error in the positive direction is within 1 LSB, the output voltage V can be kept within 1 LSB from the reference voltage.

[0032]

Also, since it is permissible to have a large error in the negative direction, resistance R can be set with a certain tolerance. Therefore, it is unnecessary to finely adjust resistance R, so

that an inexpensive D/A converter can be obtained. With regard to integration, integrator 20 can be built in or attached to the integrated circuit.

[0033]

<Second embodiment>

The second embodiment of the present invention will be explained based on Figure 3. Figure 3 is a block diagram illustrating an embodiment of the automatic control device using D/A converter 22 disclosed in the present invention. This control device can automatically set the voltage output from D/A converter 22 by providing reference voltage Va from reference voltage source 5. The differential nonlinear error in any part of D/A converter 22 is within 1 LSB in the positive direction.

[0034]

The digital data output from D/A data-increasing/decreasing unit 10 are subjected to D/A conversion conducted by D/A converter 22, which outputs voltage V. Said voltage V is converted into a digital signal by A/D converter 8 and is then input to comparator 9. Reference voltage Va is also subjected to A/D conversion conducted by A/D converter 6, and is then input to comparator 9.

[0035]

Comparator 9 compares voltage V with reference voltage Va to determine whether voltage V is higher than, lower than, or the same as reference voltage Va. If it is found by comparator 9 that voltage V is lower than reference voltage Va, D/A data-increasing/decreasing unit 10 increases the output digital data by 1. If voltage V is higher than reference voltage Va, D/A data-increasing/decreasing unit 10 decreases the digital data by 1. If signal V is the same as reference voltage Va, the digital data is not changed, and D/A data-increasing/decreasing unit 10 keeps the original value.

[0036]

For example, the initial data of D/A data-increasing/decreasing unit 10 is 0, and reference voltage Va is set to a positive value. In this case, since the output voltage of D/A converter 11 is 0, comparator 9 finds that reference voltage Va is higher. Therefore, D/A data-increasing/decreasing unit 10 increases the digital data by 1. The digital data becomes 1. D/A converter 22 outputs voltage V. If voltage V is still lower than reference voltage Va, comparator 9 will find that Va is higher than V, and D/A data-increasing/decreasing unit 10 will increase the

digital data continuously. The digital data will be increased until it is equal to or exceeds reference voltage Va.

[0037]

If output voltage V is consistent with reference voltage Va, voltage V is fixed at Va. If they are not the same and output voltage V is higher than reference voltage Va, D/A data-increasing/decreasing unit 10 vibrates the digital data near data 16 [sic]. However, since the differential nonlinear error is within 1 LSB, the change in output voltage V is small. Also, control is performed independent of the initial digital data output from D/A data-increasing/decreasing unit 10.

[0038]

In this way, highly accurate control to reference voltage Va can be realized even without using a high-performance D/A converter. The output changes significantly at segment-switching points 12-14 (see Figure 2). However, since the error is kept within the range of 1 LSB when output voltage V is controlled to match reference voltage Va, this poses no problem.

[0039]

It is also possible to properly process and control the data subjected to A/D conversion conducted by A/D converters 6, 8. For example, when reference voltage Va subjected to A/D conversion conducted by A/D converter 6 is converted to data increased several-fold, it is possible to control output voltage V of D/A converter 22 with a low reference voltage Va. Also, instead of using voltage Va as the reference for control, a current can be used as long as it can be converted into a digital signal. It is also possible to use a digital signal directly.

[0040]

<Third embodiment>

The third embodiment of the present invention is shown in Figure 4. The third embodiment is also an automatic control device using D/A converter 22. In Figure 4, the same parts as those shown in Figure 3 are represented by the same symbols, respectively, and will not be explained again. The output voltage V of D/A converter 22 is input to comparator 14. Comparator 14 compares the voltage Va of reference voltage source 5 with voltage V.

[0041]

If V is higher than Va, the output of comparator 14 becomes high level, and the digital data of counter 15 is increased by 1. As a result, the voltage V output from D/A converter 22 is

increased. The digital data is increased until voltage V exceeds reference voltage Va. When voltage V exceeds reference voltage Va, the output of comparator 14 becomes low level, and the output of the digital data of counter 15 is kept constant.

[0042]

As a result, the voltage V output from D/A converter 22 is kept constant, and a constant voltage V is applied to load 12. However, since counter 15 is controlled only in the direction of incrementing the digital data output, when a reset signal is input, the digital data becomes 0. The digital data of counter 15 is first reset to 0 by the reset signal, and then the control is started. In this way, the voltage V output from D/A converter 22 can be adjusted to reference voltage Va by being increased little by little.

[0043]

If D/A converter 22 used in this case is the conventional D/A converter shown in Figure 7, the output voltage V immediately before the segment-switching point 53 is just a little lower than reference voltage Va. When the digital data is then increased by 1, since the output voltage V undergoes a large deviation in the positive direction, output voltage V is fixed at a level far from reference voltage Va. The control accuracy becomes poor.

[0044]

However, when D/A converter 22 of the present invention is used, the deviation in the positive direction is within 1 LSB at segment-switching points 12-14, as shown in Figure 2. There is a large deviation in the negative direction at segment-switching points 12-14. Immediately before these segment-switching points, output voltage V is only a little lower than reference voltage Va. Even if the digital data is increased by 1, output voltage V is still lower than reference voltage Va. Since the linearity to the next segment-switching point is good, output voltage V is fixed at a level close to reference voltage Va.

[0045]

The control device of the present invention can control with high accuracy even without using an expensive D/A converter. The cost is therefore low. The control device disclosed in this embodiment can be used as the automatic voltage-adjusting circuit for band-pass filters or other voltage-control filters. Also, when a voltage divider (not shown in the figure) is used to divide voltage V before inputting it to comparator 14, the value of reference voltage Va can be reduced, and voltage V can be controlled. Also, when reference voltage Va is divided by a voltage divider (not shown in the figure), a low voltage V can be controlled by reference voltage Va.

[0046]

<Fourth embodiment>

The fourth embodiment of the present invention will be explained based on Figure 5. In Figure 5, the same parts as those shown in Figure 3 are represented by the same symbols, respectively, and will not be explained again. Voltage-control oscillator (VCO) 19 can control a frequency with a voltage. The oscillation frequency is increased along with the voltage. First, a reset signal is input to counter 18.

[0047]

As a result, counter 18 outputs the minimum value of the digital data. D/A converter 22 outputs the lowest voltage V. The minimum value of the digital data is set such that voltage-control oscillator 19 oscillates at the lowest frequency Fout. Oscillation frequency Fout is input to phase comparator 17.

[0048]

Phase comparator 17 compares the reference frequency Fref of reference oscillator 16 with the oscillation frequency Fout of voltage-control oscillator 19. If Fref is higher than Fout, 1 pulse is generated. When this impulse is input to counter 18, the digital data is increased by 1. In this way, the voltage V output from D/A converter 22 is increased, and the oscillation frequency Fout of voltage-control oscillator 19 is increased.

[0049]

As described above, Fout is gradually increased from the lowest oscillation frequency. When it becomes equal to Fref or higher than Fref, phase comparator 17 stops generation of the pulse, and frequency Fout is fixed. In the same way as described in the aforementioned third embodiment, the oscillation frequency will not be fixed at a level far from reference frequency Fref. Frequency Fout is fixed at a level close to reference frequency Fref.

[0050]

The control device disclosed in this embodiment is a type of PLL (phase locked loop). It can be used as the oscillator of the audio carrier for a Hi-Fi VCR. Consequently, using the inexpensive D/A converter disclosed in the present invention enables controlling voltage-control oscillator 19 with the same accuracy as that realized when using an expensive D/A converter.

[0051]

Effects of the invention

<Effect of Claim 1>

A D/A converting means with differential nonlinear error within 1 LSB is used for each segment of the D/A converter. The full scale of each segment is greater than or equal to a value calculated by dividing the full scale of the D/A converter of the upper segment by 2 raised to a power equal to the number of bits of that segment. In this way, the differential nonlinear error of the D/A converter is kept within 1 LSB in the positive direction. Since the deviation in the positive direction is small, highly accurate control can be performed. Also, since it is only necessary to eliminate deviation in the positive direction, the D/A converter becomes inexpensive.

[0052]

<Effect of Claim 2>

Since the D/A converter is inexpensive, the cost of the control device can be reduced. Since the differential nonlinear error of the D/A converter is within 1 LSB in the positive direction, a highly accurate control device can be obtained if the output of the D/A converter is controlled with respect to a reference signal.

[0053]

<Effect of Claim 3>

Since the D/A converter is inexpensive, the cost of a frequency control device for a voltage-control oscillator can be reduced. Since the differential nonlinear error of the D/A converter is within 1 LSB in the positive direction, the frequency output from the voltage-control oscillator can be controlled with high accuracy with respect to a reference frequency.

Brief description of the figures

Figure 1 is a block diagram of the D/A converter disclosed in the first embodiment of the present invention.

Figure 2 is a characteristic diagram for said D/A converter.

Figure 3 is a block diagram of the control device disclosed in the second embodiment of the present invention.

Figure 4 is a block diagram of the control device disclosed in the third embodiment of the present invention.

Figure 5 is a block diagram of the control device disclosed in the fourth embodiment of the present invention.

Figure 6 is a characteristic diagram for a conventional D/A converter.
Figure 7 is a block diagram of that conventional D/A converter.

Explanation of symbols

2	Upper D/A converting circuit
3	Lower D/A converting circuit
4	Current synthesizer
5	Reference voltage source
9	Digital signal comparator
16	Reference oscillator
17	Phase controller
15	Counter
19	Voltage-control oscillator
20	Integrator
21	Operational amplifier
22	D/A converter
R	Resistor

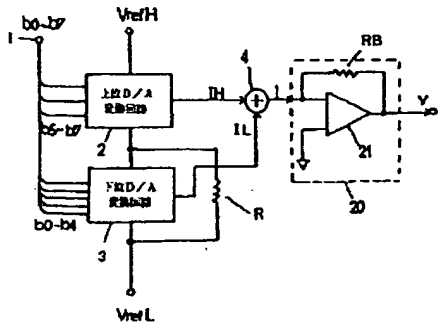


Figure 1

Key: 2 Upper D/A converting circuit
3 Lower D/A converting circuit

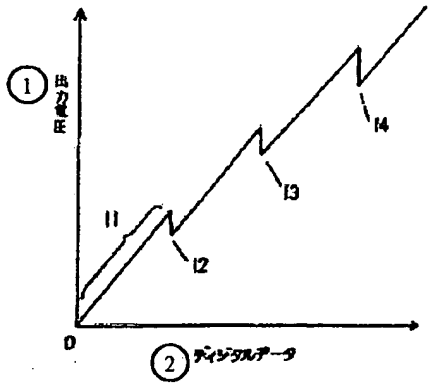


Figure 2

Key: 1 Output voltage
2 Digital data

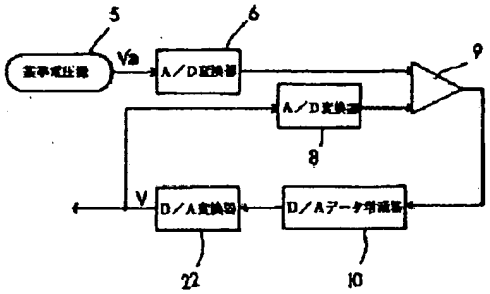


Figure 3

Key: 5 Reference voltage source
6 A/D converter
8 A/D converter
10 D/A data-increasing/decreasing unit
22 D/A converter

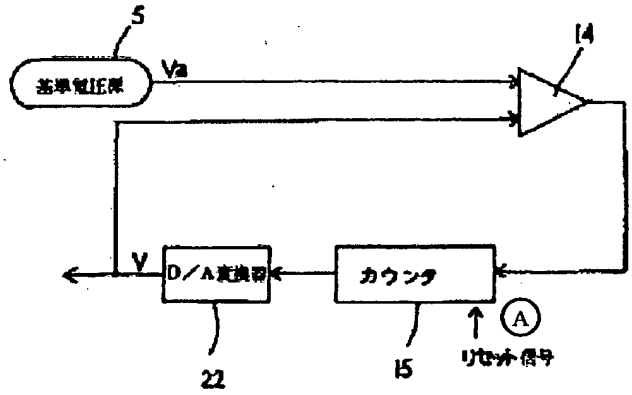


Figure 4

Key: A Reset signal
5 Reference voltage source
15 Counter
22 D/A converter

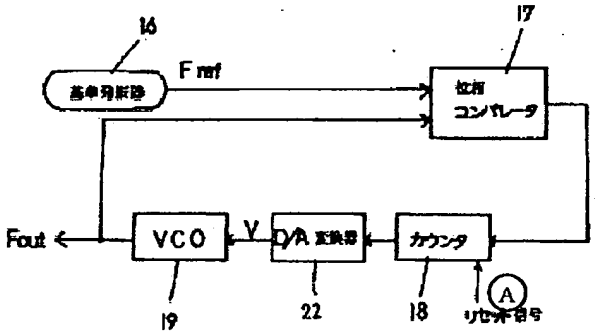


Figure 5

Key: A Reset signal
16 Reference oscillator
17 Phase controller
18 Counter
22 D/A converter

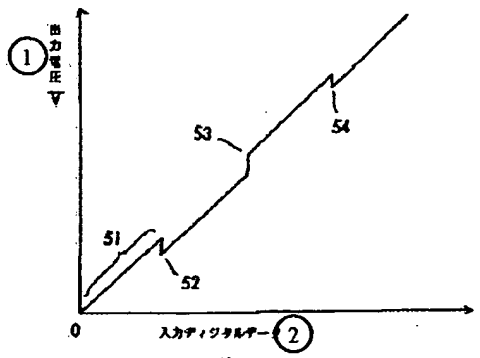


Figure 6

Key: 1 Output voltage V
2 Input digital data

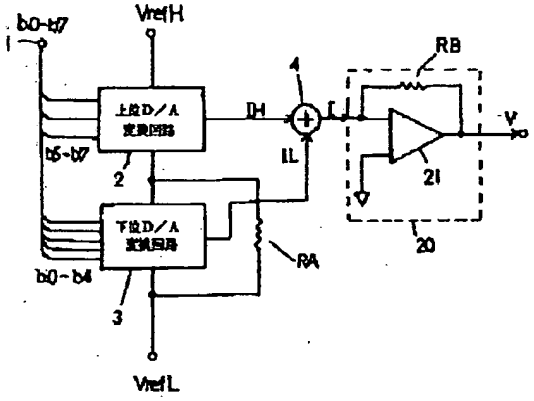


Figure 7

Key: 2 Upper D/A converting circuit
3 Lower D/A converting circuit

RALPH
MCELROY TRANSLATION
COMPANY

April 19, 2005

Re: 7037-102528

To Whom It May Concern:

This is to certify that a professional translator on our staff who is skilled in the Japanese language translated the enclosed Japanese Kokai Patent Application No. Hei 9[1997]-270707 from Japanese into English.

We certify that the attached English translation conforms essentially to the original Japanese language.

Kim Vitray
Operations Manager

Subscribed and sworn to before me this 19th day of April, 2005.

TINA WUELFING
Notary Public
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My Commission Expires
December 8, 2007

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